

The New Readout Electronic for the CERES TPC

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For the CERES beam-time in 2000 the readout system of the TPC was completely changed. A modified version of the original front-end board (see fig. 1 and [1]) and the motherboards were still used. The electronics close to the DAQ (receivers, memory modules, Compact PCI system) was replaced by newly designed boards (**F**ront **E**nd **D**igitization **C**ards). The design of these cards is based on a development for the ALICE TPC readout system. In the new setup the motherboards were used for configuring the front-end electronics and for distributing the trigger and abort signals.

Immediately after receiving a trigger signal the SCA (Switched Capacitor Array) on the front-end board starts to sample the 16 outputs of the amplifier in parallel. Up to 250 individual time samples for each channel can be stored to allow three-dimensional reconstruction of the tracks. The sampling phase is followed by the readout phase in which the stored analog values are dumped in a time-wise order. During the readout phase the output signal of the SCA has a maximum swing (AC component) of 2 V and a baseline (DC component) that can be adjusted online via a DAC on the front-end board.

The digitization and further processing of the TPC signals is done on the FEDC-boards. These boards are realized as 9U VXI devices which can contain up to 48 readout channels. Each readout channel comprises a 10-bit ADC and a digital chip for signal processing (a modified version of the ALTRO chip for the ALICE TPC [2]) and processes the data from one front-end board. After converting the analog signal the data stream is demultiplexed according to the 16 channels of the preamplifier. The resulting 16 data streams are processed in parallel inside the ALTRO chip. The data is represented and processed only with the 9 MSB, resulting in a loss of 1 bit in resolution. Therefore, the signal is described by a 9 bit code (0 – 511).

In the following processing steps the polarity of the signal is changed and the baseline is subtracted. After this subtraction the signal should be contained in the first half of the 9 bit range. Therefore the most significant bit can be

omitted reducing the signal representation to 8 bit codes. Finally the signal undergoes zero suppression. Samples with a value smaller than a constant threshold (8 bit) are rejected. When a sample is found to be above the threshold, it is considered as the start of a pulse (cluster) and stored in the central memory of the FEDC.

Inside the FEDC an event is stored in memory as a back-linked structure. Due to reordering of samples between accepted clusters, the timing information is lost during the zero-suppression process. This requires the addition of two additional words – the time-stamp and the cluster-length. The cluster-length corresponds to the total number of samples plus the time-stamp and the cluster-length. The time-stamp gives the (sample-)position of the last sample in the cluster relative to the trigger signal. This cluster structure (sample values + time-stamp + cluster-length) is repeated for each accepted cluster in a specific channel. For each channel up to 250 time samples can be accepted.

Because each ALTRO chip processes data coming from 16 TPC-channels with a maximum of 250 time samples, it was not possible to provide enough memory inside the chips to hold pedestal values for all samples. Instead, a scheme using a look-up table was implemented. The look-up table contains 250 7 bit words. The index (the linenum-ber) of this table corresponds to the sample number. The entries are the addresses of the data-buffers which contain the pedestal values. This means, 128 pedestal values can be assigned to each channel.

Three FEDC boards are combined in one VME-crate. Each of these boards is connected to 40 front-end cards, i. e. processing the data from 640 TPC pads. In total, 24 FEDC boards are needed to read out the whole TPC. The connection between these crates and the readout PCs (cf. [3] for more details) are realized with National Instruments' MXI-bus. MXI-bus is a general purpose, 32-bit multi-master system bus on a cable. It provides a way of controlling VXI systems using commercially available desktop computers and workstations. In CERES a PCI-VME bridge is used. This configuration consists of a PCI card (plugged in the readout PCs), MXI-2 bus and a MXI-VME interface card which is plugged into the VME-crate for the FEDC cards. Data and control signals are converted on the PCI board and sent over the MXI bus, which is essentially the VME on a cable, into the MXI-VME interface board. The 6U MXI-VME interface board in conjunction with the MXI-2 cable enables data transfers up to 38 MBytes/s using D64 transfers.

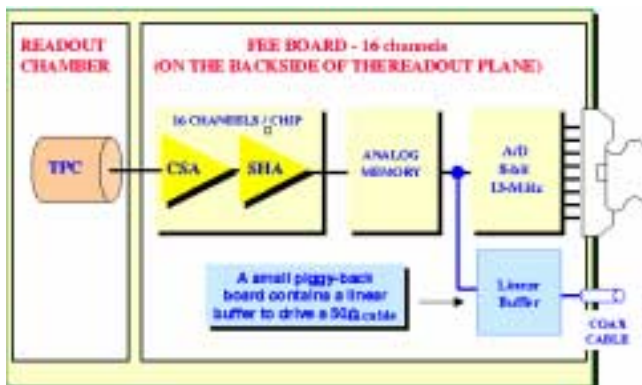


Figure 1: The modified FEE card.

References

- [1] R. Baur *et al.*, GSI Scientific Report 1998 p. 190.
- [2] ALICE Collaboration, Technical Design Report, CERN/LHCC 2000-001
- [3] D. Miśkowiec *et al.*, this Report